AMENDMENTS TO THE CLAIMS

1. (Currently amended) A non-volatile semiconductor memory cell structure, comprising:

a substrate having a shallow first-type well layer, a second-type well layer and a deep first-type well layer, wherein the deep first-type well layer is at a greater depth than the shallow first-type well layer and the second-type well layer is between the shallow first-type well layer and the deep first-type well layer;

a plurality of stack gates above the shallow first-type well layer of the substrate; and

a plurality of source terminals and drain terminals between the stack gates, wherein depth of the source terminal is long enough to pass through the shallow first-type well layer and connect with the second-type well layer, and both the source terminals and the drain terminals are second-type-doped regions[.]; wherein each source terminal further includes:

a lightly doped region close to the substrate surface; and

a heavily doped region underneath the lightly doped region but in connection with the lightly doped region such that the heavily doped region passes through the shallow first-type well layer in connection with the second-type well layer;

wherein both the lightly doped region and the heavily doped region are second-type-doped regions with a dopant concentration greater in the heavily doped region than the lightly doped region.

2. (Original) The memory cell structure of claim 1, wherein the shallow first-type well layer and the deep first-type well layer are P-doped layers and the second-type well layer, the source terminals and the drain terminals are N-doped layers.

3. (Original) The memory cell structure of claim 1, wherein the shallow first-type well layer and the deep first-type well layer are N-doped layers and the second-type well layer, the source terminals and the drain terminals are P-doped layers.

4. (Original) The memory cell structure of claim 1, wherein each stack gate further includes:

a first dielectric layer over the substrate;

a floating gate over the first dielectric layer;

a second dielectric layer over the floating gate; and

a control gate over the second dielectric layer.

5. (Original) The memory cell structure of claim 4, wherein the second dielectric layer includes an oxide/nitride/oxide composite layer.

6. (Original) The memory cell structure of claim 1, wherein each stack gate includes:

a first dielectric layer over the substrate;

a trap layer over the first dielectric layer;

a second dielectric layer over the trap layer; and

a control gate over the second dielectric layer.

7. (Original) The memory cell structure of claim 6, wherein the first dielectric layer and the second dielectric layer are silicon oxide layers and the trap layer is a silicon nitride layer.

8. (Canceled)

9. (Original) The memory cell structure of claim 1, wherein

the drain terminal and the shallow first type well layer are shorted.

10. (Currently amended) The memory cell structure of claim 9, wherein a metal contact ~~is located where~~ penetrates through a junction between the drain terminal and the shallow first type well layer so that the drain terminal and the shallow first type well layer ~~is~~ are shorted.

11. (Currently amended) The memory cell structure of claim 9, wherein the a metal contact is located ~~where is across~~ to butt an exposed surface of the drain terminal and the shallow first type well layer so that the drain terminal and the shallow first type well layer ~~is~~ are shorted.